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EXAMINER	
STEVENSON, ANDRE C	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 09/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/774,362	MATSUO, YOSHIHIDE	
	Examiner	Art Unit	
	Andre' C. Stevenson	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *June 26, 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *20-31* is/are withdrawn from consideration.

5)☒ Claim(s) *4,7 and 10* is/are allowed.

6)☒ Claim(s) *1,3,5,6,8,9 and 11-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims #1, 2, 3, 5, 6, 8, 9, 17, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Siniaguine (U.S. Pat. No.6,664,129 B2, Patented 12/16/03, Filed 12/12/02), and in view of Komura et al. (U.S. Pat. No.5,423,941, Patented 06/13/95, Filed 11/17/93).

Siniaguine substantially shows the claimed invention, as shown in figures 1-13 and corresponding text, in a similar method, **pertaining to claims #1, 17, 18 and 19**, a manufacturing method for a semiconductor device comprising: a hole **(item 124)** portion formation step for forming hole portions whose entire width is substantially identical to the width of the opening portion in a part of the active surface **(item 110 f)** side of the substrate **(item 110)** on which electronic components are formed **(column 2, lines 7-11 and lines 17-31)**; a connecting terminal **(item 150)** formation step for forming connecting terminals that serve as the external electrodes of the electronic circuits by burying metal in the hole portions **(column 2, lines 42-54)**; and an exposure step for exposing a part of the connecting terminals by carrying out processing on the back surface of the substrate **(column 1, lines 24-35; column 3, lines 13-29)**. ***Pertaining to claim #2,*** Siniaguine shows, a manufacturing method for a connection

terminal formation step for forming connection terminals that serve as the external electrodes of the electronic circuits by burying metal in the hole portions **(column 2, lines 42-54)** and an exposure step for exposing a part of the connecting terminals by carrying out processing on the back surface of the substrate **(column 3, lines 13-29)**. ***Pertaining to claim #3,*** Siniaguine shows, a manufacturing method for a semiconductor device, wherein the exposure step is a step in which a part of the connecting terminals is exposed without changing the shape of the connecting terminals **(column 3, lines 45-52)**. ***Pertaining to claim #5,*** Siniaguine shows, a manufacturing method for a semiconductor device comprising: a concavo-convex shape formation step for forming a concavo-convex shape **(item 124c)** on a part of the active surface **(item 104)** side of the substrate **(item 110)** on which the electronic circuits are formed **(column 2, lines 7-11)**; a hole formation step for forming hole portions by etching the area in which the concavo-convex shape **(item 124c)** has been formed, whose entire width is substantially equal to the width of the area on which the concavo-convex shape **(item 124c)** has been formed and whose bottom surface has a shape substantially identical to the concavo-convex shape **(item 124c) (column 2, lines 17-31)**; a connecting terminal **(item 150)** formation step for forming the connecting terminals that serve as the external electrodes of the electronic circuits by burying metal in the hole portions; and an exposure step for exposing a part of the connecting terminals by carrying out processing of the back surface of the substrate **(column 2, lines 42-54)**. ***Pertaining to claim #6,*** Siniaguine shows, a manufacturing method for a semiconductor, wherein the exposure step is a step in which a part of the connecting terminals is exposed without changing the shape of the connecting terminal **(column 3, lines 13-28)**. ***Pertaining to claim #8,*** Siniaguine shows, a manufacturing method for a semiconductor device comprising: a mask formation step for forming a mask

having a plurality of holes **(item 124)** in the hole formation area set in a part of the active surface **(item 10f)** side of the substrate **(item 110)** on which the electronic circuits are formed **(column 2, lines 17-31)**; a connecting terminal **(item 150)** formation step for forming connecting terminals that serve as the external electrodes for the electronic circuits **(item 204&208)** by burying metal in the hole portions **(column 5, lines 25-33)**; and an exposure step for exposing a part of the connecting terminals by carrying our processing on the back surface of the substrate **(column 1, lines 24-35; column 3, lines 13-29).** The Examiner notes that the prior art fails to mention explicitly a "plurality of holes". However, it does state in column 2, line 24-26, that one or more openings (item 124) are formed, and that in column 2, line 24-26, that openings 124 is formed by a mask. The Examiner takes the position that this is the equivalent to a mask with a plurality of holes. ***Pertaining to claim #9,*** Siniaguine shows, a manufacturing method for a semiconductor device wherein the exposure step is a step in which a part of the connecting terminals is exposed without changing the shape of the connecting terminals **(column 3, lines 45-52).**

Siniaguine fails to show, **with respect to claim #1**, a curved surface formation step using isotropic etching for curving the bottom surface of the hole portion while maintaining the width of the bottom surface in the hole portions substantially identical to the width of the opening portion. Siniaguine also fails to show, **pertaining to claim #2**, a hole portion formation step for forming hole portions whose entire width is substantially identical to the width of the opening portion in a part of the active surface side of the substrate on which electronic components are formed a curved surface formation step for curving the bottom surface of the hole portion while

maintaining the width of the bottom surface in the hole portions substantially identical to the width of the opening portion, wherein the curved surface formation step is a step in which the bottom surface of the hole portion is formed into an approximately semispherical shape by isotropic etching. Finally, Siniaguine fails to show, **pertaining to claim #8**, a formation step for forming hole portions whose entire width is substantially identical to the width of the hole formation area and whose bottom surface has a concavo-convex shape by etching the substrate through each of the holes formed in the mask using an etching method in which the holes widen slightly in the surface direction of the substrate.

Komura teaches, in a similar method for forming deep trenches on a surface of a semiconductor substrate, pertaining to **claim #1**, a curved surface formation step using isotropic etching for curving the bottom surface of the hole portion while maintaining the width of the bottom surface in the hole portions substantially identical to the width of the opening portion **(column 1, lines 41-67).** The Examiner notes that Komura does not state explicitly that the width of the bottom surface in the hole portions are substantially identical to the width of the opening portions. However, Komura teaches a method for isotropic etching, using a gas composition that provides deep trenches with good reproducibility and with good configuration, preserving a slight taper of trench sidewall at an angel near 90^0. The Examiner takes the position that Komura's method of controlling the angle of the sidewalls, shows not only the capacity to maintain the widths of the trenches, but also teaches widths that are substantially the same. For this reason, the Examiner takes the position that the method taught by Komura, is equivalent the method presented in the claim language. ***Pertaining to claim #2,*** Komura shows, manufacturing

method for a semiconductor device comprising: a hole portion formation step for forming hole portions whose entire width is substantially identical to the width of the opening portion in a part of the active surface side of the substrate on which electronic components are formed **(column 1, lines 13-26)** a curved surface formation step for curving the bottom surface of the hole portion while maintaining the width of the bottom surface in the hole portions substantially identical to the width of the opening portion **(fig. 1a; column 1, lines 41-67)**, wherein the curved surface formation step is a step in which the bottom surface of the hole portion is formed into an approximately semispherical shape by isotropic etching **(column 1, lines 41-67).** ***Pertaining to claim #8,*** Komura teaches a concavo-convex shape hole formation step for forming hole portions whose entire width is substantially identical to the width of the hole formation area and whose bottom surface has a concavo-convex shape by etching the substrate through each of the holes formed in the mask using an etching method in which the holes widen slightly in the surface direction of the substrate **(fig. #1; column 1, lines 13-26 and lines 41-67)**;

It would have been obvious to one having ordinary skill in the art, at the time the invention was made, with respect to **claims #1, 2 and 8**, to include a formation step for forming hole portions whose entire width is substantially identical to the width of the opening portion in a part of the active surface side of the substrate on which electronic components are formed a curved surface formation step for curving the bottom surface of the hole portion while maintaining the width of the bottom surface in the hole portions substantially identical to the width of the opening portion, wherein the curved surface formation step is a step in which the bottom surface of the hole portion is formed into an approximately semispherical shape by

isotropic etching, in the method of Siniaguine, as taught by Komura, with the motivation, (Komura, column 1, line 6-12) that forming deep trenches, by way of dry etching a semiconductor substrate, is particularly useful for manufacturing an article made from Si, such as semiconductor DRAM.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 11, 12, 13, 14, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Siniaguine (U.S. Pat. No.6,664,129 B2, Patented 12/16/03, Filed 12/12/02) as applied to claims 1,3, 5, 6, 8, 9 and 17-19 above, in view of Ormond et al. (U.S. Pat. No.5,521,125, Patented 05/28/96, Filed 10/28/94).

Siniaguine substantially shows the claimed invention, as shown in figures 1-13 and corresponding text, in a similar method, **pertaining to claim #11,** a stacking step for stacking an identical type of the semiconductor chips or different types of the semiconductor chips **(fig. 4; column 3, lines 54-67)**; and a bonding step for bonding together the connecting terminals formed on the stacked semiconductor chips **(column 3, lines 54-67; column 4, lines 1-3).** ***Pertaining to claim #12,*** Siniaguine shows, a mounting step for mounting one or a plurality of the identical type of semiconductor chips or the different types of semiconductor chips on the substrate on which the connecting portion is formed **(fig. 4; column 3, lines 54-67)**; and a

bonding step for bonding together the connecting terminals formed on the stacked semiconductor chips or bonding the connecting portion and the connecting terminal **(column 3, lines 54-67; column 4, lines 1-3). Pertaining to claim #13,** Siniaguine shows, a stacking step for stacking an identical type of the semiconductor chips or different types of the semiconductor chips **(fig. 4; column 3, lines 54-67)**; and a bonding step for bonding together the connecting terminals formed on the stacked semiconductor chips **(column 3, lines 54-67; column 4, lines 1-3).** ***Pertaining to claim #14,*** Siniaguine shows, a mounting step for mounting one or a plurality of the identical type of semiconductor chips or the different types of semiconductor chips on the substrate on which the connecting portion is formed **(fig. 4; column 3, lines 54-67)**; and a bonding step for bonding together the connecting terminals formed on the stacked semiconductor chips or bonding the connecting portion and the connecting terminals **(column 3, lines 54-67; column 4, lines 1-3). Pertaining to claim #15,** Siniaguine shows, a stacking step for stacking an identical type of semiconductor chips or different types of the semiconductor chips **(fig. 4; column 3, lines 54-67)**; and a bonding step for bonding together the connecting terminals formed on the stacked semiconductor chips **(column 3, lines 54-67; column 4, lines 1-3).** ***Pertaining to claim #16,*** Siniaguine shows, a mounting step for mounting one or a plurality of the identical type of semiconductor chips or the different types of semiconductor chips on the substrate on which the connecting portion is formed **(fig. 4; column 3, lines 54-67)**;; and a bonding step for bonding together the connecting terminals formed on the stacked semiconductor chips or bonding the connecting portion and the connecting terminals **(column 3, lines 54-67; column 4, lines 1-3).**

Siniaguine fails to show, with respect to **claims #11 and 12**, a manufacturing method for a semiconductor device comprising: a dicing step for dicing the semiconductor device formed by the manufacturing method for a semiconductor device according to claim #1 into individual semiconductor chips. Also, Siniaguine fails to show, with respect to **claims #13 and 14,** a manufacturing method for a semiconductor device comprising: a dicing step for dicing the semiconductor device formed by the manufacturing method for a semiconductor device according to claim 5 into individual semiconductor chips. Finally, Siniaguine fails to show, with respect to **claims #15 and 16,** a manufacturing method for a semiconductor device comprising: a dicing step for dicing the semiconductor device formed by the manufacturing method for a semiconductor device according to claim 8 into individual semiconductor chips.

Ormond teaches, in a similar method, **pertaining to claims #11 and 12,** a manufacturing method for a semiconductor device comprising: a dicing step for dicing the semiconductor device formed by the manufacturing method for a semiconductor device according to claim 1 into individual semiconductor chips **(column 1, lines 4-7; column 4, lines 59-67; column 5, lines 1-4).** Ormond teaches also, in a similar method, **pertaining to claims #13 and 14,** a manufacturing method for a semiconductor device comprising: a dicing step for dicing the semiconductor device formed by the manufacturing method for a semiconductor device according to claim 5 into individual semiconductor chips **(column 1, lines 4-7; column 4, lines 59-67; column 5, lines 1-4).** Finally, Ormond teaches, in a similar method, **pertaining to claims #15 and 16,** a manufacturing method for a semiconductor device comprising: a dicing step for dicing the semiconductor device formed by the manufacturing method for a

semiconductor device according to claim 8 into individual semiconductor chips **(column 1, lines 4-7; column 4, lines 59-67; column 5, lines 1-4).**

It would have been obvious to one having ordinary skill in the art, at the time the invention was made, with respect to **claims #11 and 12**, to include a dicing step for dicing the semiconductor device formed by the manufacturing method for a semiconductor device according to claim #1, into individual semiconductor chips, in the method of Siniaguine, as taught by Ormond, with the motivation that in order to present or stack the devices for production or assembly, they must be separated. The conventional method for separating chips is dicing.

It would have been obvious to one having ordinary skill in the art, at the time the invention was made, with respect to **claims #13 and 14**, to include a dicing step for dicing the semiconductor device formed by the manufacturing method for a semiconductor device according to claim 5 into individual semiconductor chips, in the method of Siniaguine, as taught by Ormond, with the motivation that in order to present or stack the devices for production or assembly, they must be separated. The conventional method for separating chips is dicing.

It would have been obvious to one having ordinary skill in the art, at the time the invention was made, with respect to **claims #15 and 16**, to include a dicing step for dicing the semiconductor device formed by the manufacturing method for a semiconductor device according to claim 8 into individual semiconductor chips in the method of Siniaguine, as taught

by Ormond, with the motivation that in order to present or stack the devices for production or assembly, they must be separated. The conventional method for separating chips is dicing.

Allowable Subject Matter

Claim #4

- ✓ A first etching step for etching the back surface of the substrate until the thickness of the substrate is approximately slightly thicker than the burying depth of the connecting terminals.

Claim #7

- ✓ A first etching step for etching the back surface of the substrate until the thickness of the substrate is approximately slightly thicker than the burying depth of the connecting terminals.

Claim #10

- ✓ A first etching step for etching the back surface of the substrate until the thickness of the substrate is approximately slightly thicker than the burying depth of the connecting terminals.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure; Turner et al. (U.S. Pat. No. 6,794,272), Kuesters et al. (U.S. Pat. No. 5,025,295), Yoshimura et al. (U.S. Pat. No. 6,706,546 B2.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre' Stevenson whose telephone number is (571) 272 1683. The examiner can normally be reached on Monday through Friday from 7:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt, can be reached on (571) 272 1873. The fax phone number for the organization where this application or proceeding is assigned is (703) 308 7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308 0956. Also, the proceeding numbers can be used to fax information through the Right Fax system;

(703) 872-9306

Andre' Stevenson

08/06/05

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER